

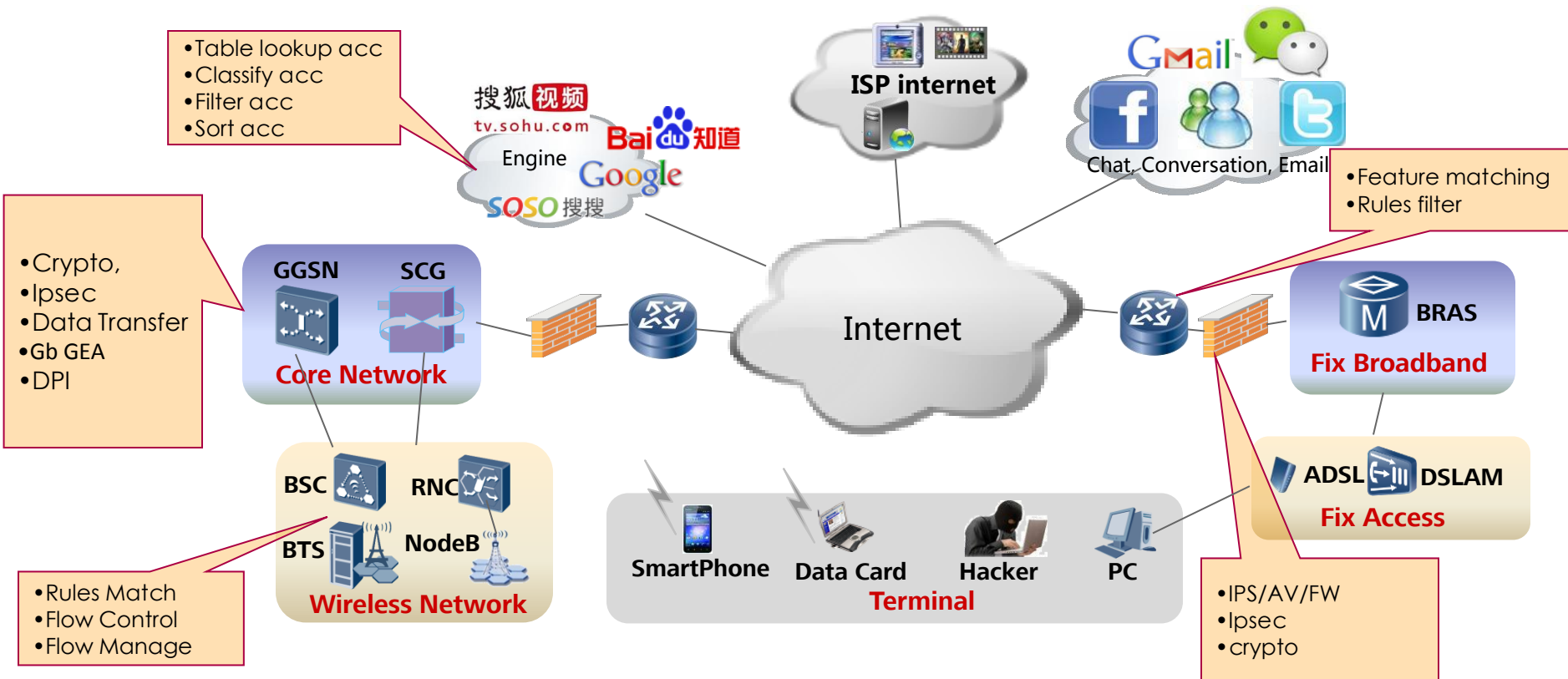
Virtualization of Crypto Accelerator

Huawei UVP

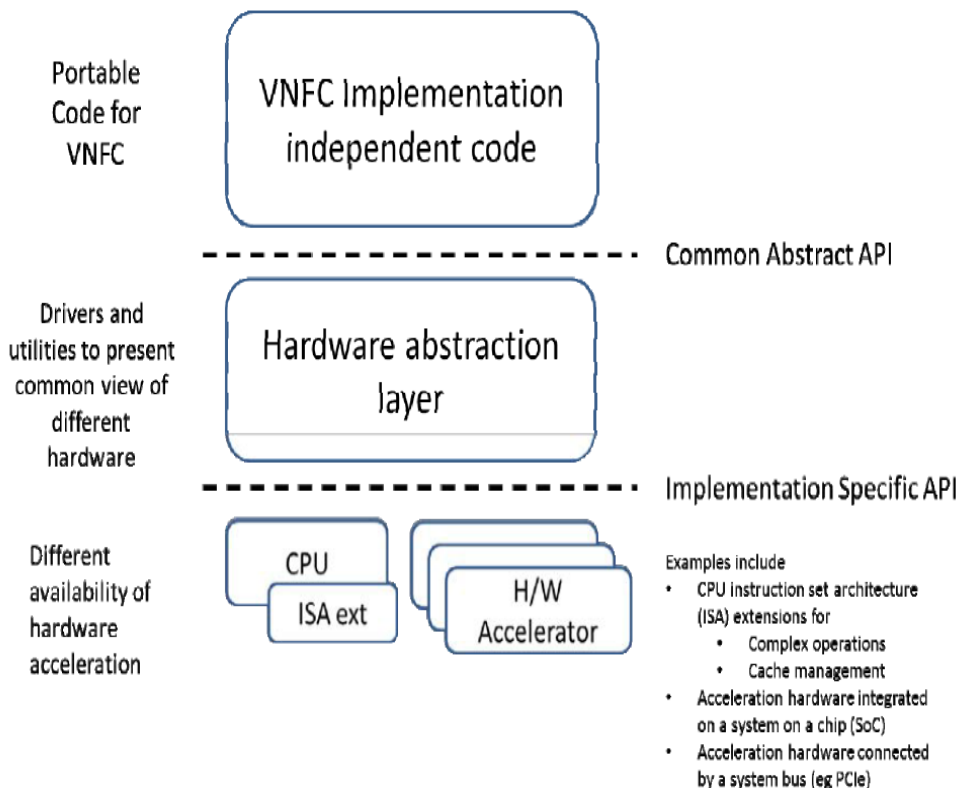
8/17/2015

www.huawei.com

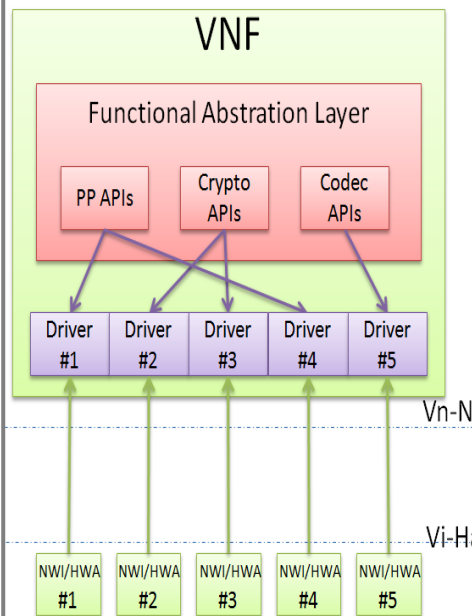
Scenarios of Hardware Acceleration



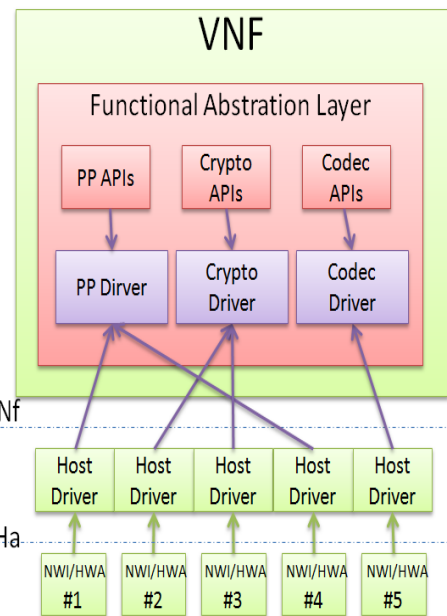
Abstract model of Accelerators (NFV)



"Pass-Through" Model



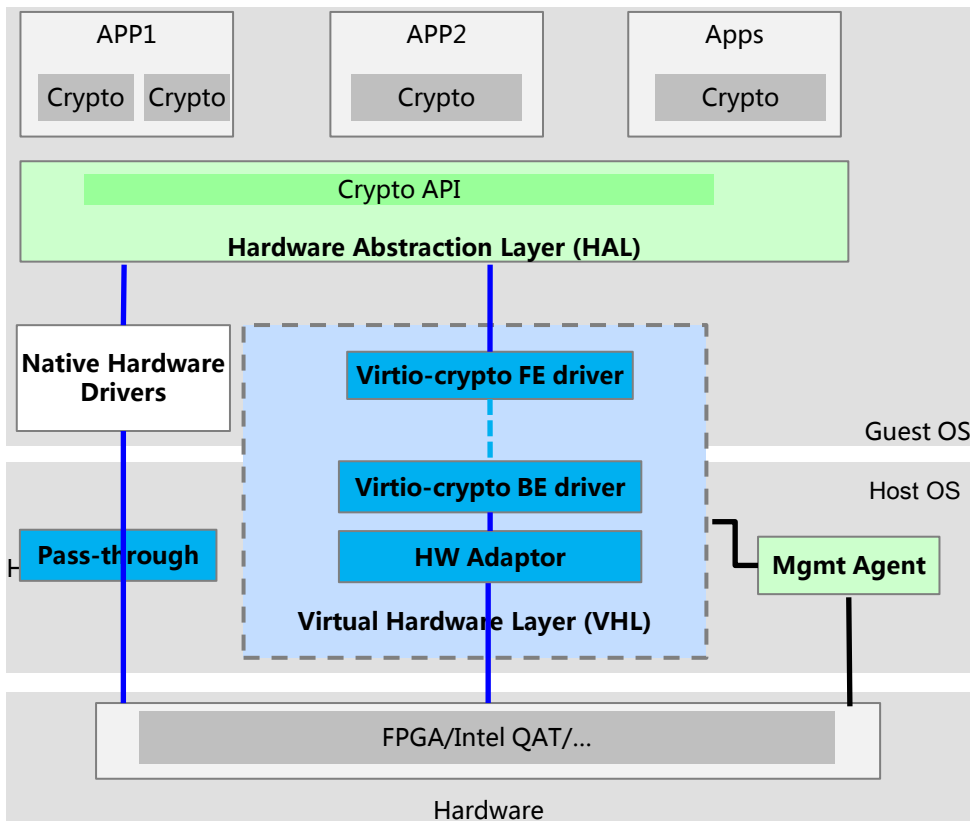
"Fully Intermediated" Model



https://wiki.opnfv.org/dpacc/dpacc_project_proposal

Note: the original figure forwarded from ETSI GS NFV-INF 003 V1.1.1 (2014-12)

Virtualization of Crypto Accelerator



1. HAL

Provide acceleration APIs and runtimes

2. VHL

Provide virtual accelerators:

- 1) virtio-crypto FE driver
- 2) virtio-crypto BE driver
- 3) HW Adaptor : support different crypto accelerators

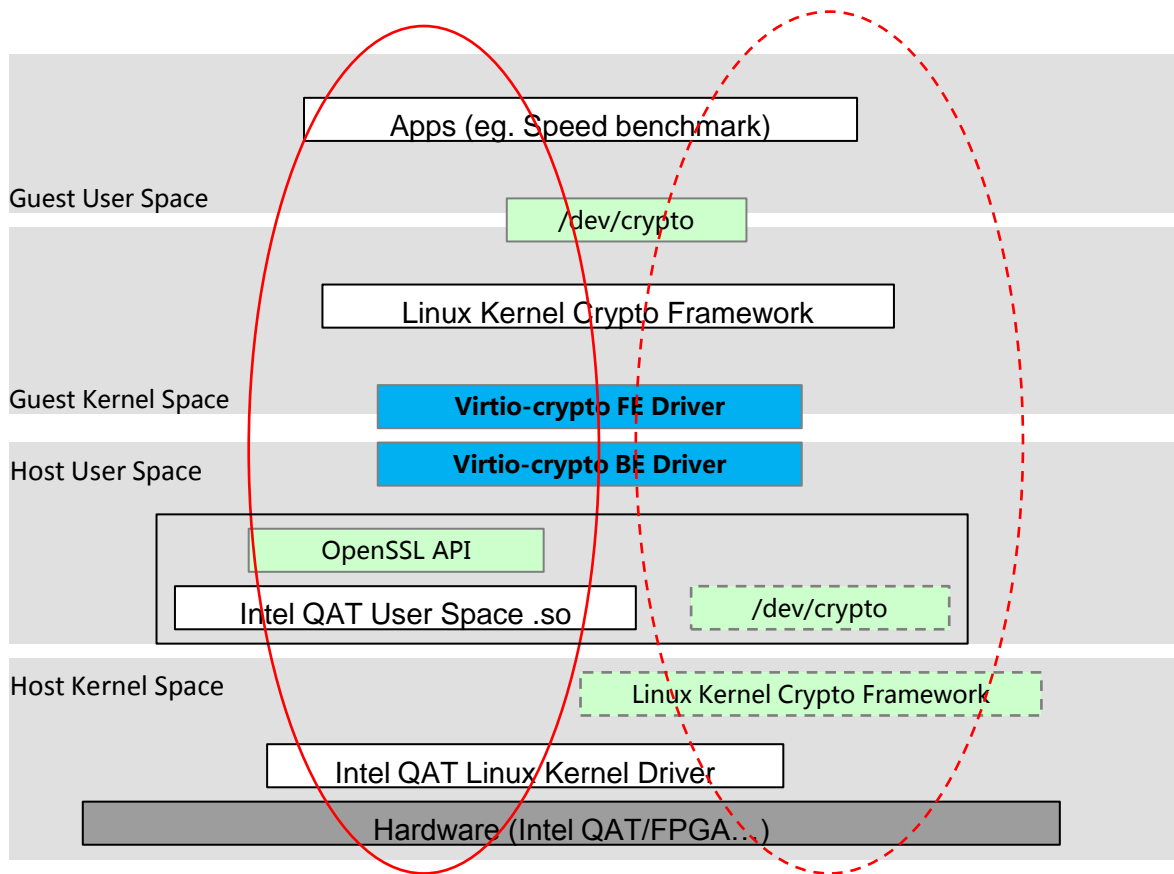
3. Pass-through

Accelerator pass-through

4. Mgmt Agent

Accelerator management

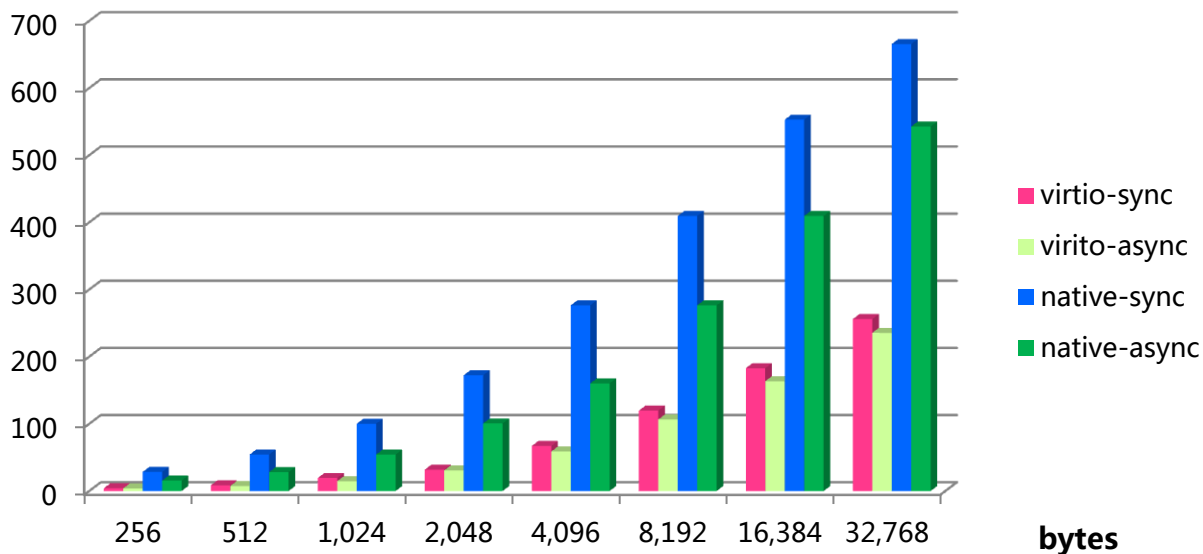
Flow of Prototype



Note: The left ellipse is today's demo scheme

Performance

Crypto-dev speed/async-speed benchmark (Mb/sec) AES-128-CBC



• Hardware

1) Intel(R) Xeon(R) CPU E5-2620 v3 @ 2.40GHz

2) Intel QAT Coletto Creek PCIe DH895xCC SKU2

• Software

Guest: Suse11.3 with 8 GB memory, 8vcpu

Host: KVM 3.12, QEMU 2.4-rc3

TODO:

1. Performance optimization: virtio-crypto-dataplane, batch processing, etc.
2. Other crypto APIs support
3. Virtio-crypto upstream